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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
87552.070100/SE-1486IP.A

Total Pages in this Submission

jc544 U.S. PTO 04/19/00

jc525 U.S. PTO 09/552117 04/19/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

and invented by:

Bogdan M. Duduman

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **12** pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☒ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets 3
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	15	- 20 =	0	x	$18.00	$0.00
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Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$690.00

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Thomas R. FitzGerald

Signature

Dated: **April 19, 2000**

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Bogdan M. Duduman**			Docket No. **87552.070100/SE-1486IP.A**
Serial No. **TBA**	Filing Date **Herewith**	Examiner **Unknown**	Group Art Unit **Unknown**

Invention: **ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS**

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Bogdan M. Duduman**			Docket No. **87552.070100/SE-1486IP.A**
Serial No. **TBA**	Filing Date **Herewith**	Examiner **Unknown**	Group Art Unit **Unknown**

Invention: **ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS**

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ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

Background

This invention relates to a power monitor circuit and in particular to a circuit for monitoring the power of a personal computer. This patent is a conversion of U.S. Provisional Application SN 60/130,828 filed April 23, 1999.

Personal computers have circuits that monitor control the power supplied to different parts of the computer. Some parts, such as memory, require a different voltage than other parts, such as the microprocessor. In order to conserve power and lengthen the life of the integrated circuits, it is economical to reduce the power available to components when the computer is inactive. Most computers have a power saving feature that reduces the power consumption after a predetermined idle time. The operator may have control of that time. During the power down time, minimal power is supplied to the computer. In theory, one only needs to supply enough power to sense when the user returns to resume usage (full power required). Despite the speed of integrated circuits, there remains a finite amount of time for the power supplies to reach their nominal operating levels. If the computer begins operation before the input power supplies reach their nominal operating levels, computations and operations performed by the computer may be erroneous. Such premature operation may cause errors in operation that, in return, could cause the computer to fail and shut down. Then, the user will have to restart the computer or perhaps repair it as well.

The power management feature contributes to overall efficiency, saves energy and reduces the cost of operating the computer. As personal computers become more sophisticated, the power up and power down monitoring circuits have likewise grown in

sophistication. More sophisticated circuits are required because the computer uses numerous voltages. Some of the primary voltages used in a computer are 12 volts, 5 volts, and 3.3 volts. These are supplied from an AC/DC converter to other devices and chips within the computer. As such, the motherboard on a computer requires still further voltages derived from the primary voltages for operating memory chips, graphics chips and clock chips. Nevertheless, all of those derived voltages are derived from the three primary voltages of 12, 5, and 3.3 volts.

It is important that the various devices be powered up and powered down in the manner specified by the computer manufacturer. Unless the power up and power down operations are controlled and there is sufficient power, valuable data may be lost or the system may conflict with itself and crash.

For proper operation, the three primary voltages must be at or about 90% of their expected operating level. Microprocessor vendors, such as Intel Corporation, specify that the microprocessor and the motherboard will be fully operational after a predetermined time window. That time window is currently set to about 100 ms. In order to assist PC manufacturers, Intel also specifies that the 3.3 and 5.0 volt supplies must reach 90% of their value in less than 40 ms. The problem faced by computer manufacturers is how to monitor the primary voltages to determine when the voltages derived from the primary voltages can be created.

Some manufacturers have proposed using three power supply monitor chips, one for each primary voltage. That is a straightforward approach, but it multiplies the number of power supply monitors to match the three primary voltages. Still others have suggested using a single chip for monitoring the power supplies and on that single chip include three primary voltage monitor circuits, i.e., one circuit for each of the three primary voltages.

Summary

The invention improves upon the solutions of the prior art by providing a single power monitor-integrated circuit with a single input primary voltage pin. The invention accomplishes this desirable result by using the inherent features of the power supply. The power supply is made to exacting specifications. The power supply will drive the 3.3 volt and 5.0 volt supplies to reach 90% of their values within 40 ms after the 12 volt supply reaches 90% of its value. A suitable time delay circuit 25 delays switching the 3.3 volt and 5 volt dual supplies from the standby voltage supply to the active voltage supply until after the primary 3.3 volt and 5 volt are operating.

The invention provides an integrated circuit that monitors and controls power from a computer ATX power supply. A conventional ATX power supply generates a plurality of different output voltages but the 3.3, 5, and 12 volt outputs are derived from a single power transformer. The integrated circuit includes one input pin that provide input means for receiving a representative power output (12 volt in this case) from the ATX power supply. The integrated circuit also includes a conventional linear power controller circuit for controlling each of its power outputs. A comparator circuit compares a signal representative of the primary power voltage to a reference signal. A voltage divider provides one input to the comparator and the other input is provided by a threshold reference source. When the divided signal exceeds the threshold, the comparator output a signal indicative of the results. That signal means that the primary power supply has reached at least 90% of its targeted value. The output of the comparator then triggers a timing circuit. The switchover of the power outputs controlled by the integrated circuit from the standby input supply to the main ATX outputs is delayed by the timing circuit for a set time that corresponds to the timing specifications of the ATX supply. Those specifications require that the primary power sources be at their respective voltage levels within a very carefully controlled time, typically 40 milliseconds. The timing circuit is set to a delay time that equals or exceeds the ATX specification. After the time delay expires, the invention generates a power up signal. At

that time the power outputs controlled by the integrated circuit are switched to the primary input power sources, such that at the end of the 100 millisecond period, the computer may enter the active state of operation.

Drawings

Figure 1 is a high level schematic of the power distribution system in a computer.

Figure 2 is schematic of the comparator circuit of the invention.

Figure 3 is a schematic of an integrated circuit using the power management circuit of the invention.

Figure 4 is a graph showing a soft start interval in a sleep state with all outputs enabled.

Figure 5 is a graph showing a soft start interval in an active state.

Detailed Description

With reference to Fig. 1, there is shown a high-level circuit schematic of a portion of a personal computer. The ATX AC/DC power supply 10 includes a transformer and DC to DC converter circuitry. The power supply 10 includes a connection at its input to a source of alternating current. Its nine outputs include a 5-volt standby output and three primary voltage outputs of 12, 5 and 3.3 volts. The outputs from the ATX power supply are tightly coupled to one another. Indeed, they are all derived from the same AC transformer. Once the primary 12 volt power supply passes 90% of its nominal setting, the 5 volt and 3.3 volt supply will equal or exceed 90% of their nominal settings no later than the end of the 40-ms window. In effect, it is possible to use the 12 volt primary power voltage as a proxy for the other primary voltages. It is not necessary to actually monitor the 5 and the 3.3 voltages because they are related to the 12 volt supply. Instead, one monitors the 12 volt supply for overall compliance. Once the 12 volt supply is in compliance, the 5 and 3.3 volt supplies will be in compliance by the end of the 40-ms window.

The invention is implemented by incorporating a comparator circuit 22 into the power

monitor of the integrated circuit 20. The comparator circuit 22 is a resistor divider network that includes resistors R1 and R2. See Figure 2. Resistors are chosen of sufficient value so that the voltage into the comparator 24 is divided to be within the range of the 5 volt standby power supply. The voltage V_{REF} input to comparator 24 is derived from the 5 volt standby power supply. The maximum reference level is set to 90% of the nominal value, i.e., 90% of 12 v = 10.8 volts. In the preferred embodiment, the reference voltage is approximately 1.2 volts and the voltage divider is a 9-to-1 divider. Thus, when there are 10.6 volts across resistor R2, the inputs to the comparator are equal and the output signal at terminal 27 of the comparator is high indicating that the voltage V_{12} is approximately 90% of its nominal value. The high signal at terminal 27 is transmitted via control line 32 to a circuit that creates the derived voltages. The high output of the comparator 24 is delayed by time delay circuit 25. The control signal indicates that the power supplies for 5, 3.3 and 2.5 volts are now at suitable levels for use to create the derived voltages.

Turning to Figure 3, further details of the invention are provided. The 12 volt primary power supply signal from the power supply 10 is supplied to the motherboard and is monitored via line 301. That line provides an input to a voltage divider (not shown; see Fig. 2) that is contained inside the monitor integrated circuit 22. The power monitor integrated circuit 22 includes a timing circuit (not shown; see Fig. 2) that measures the time from when the 12 volt supply equals or exceeds 90% of its nominal value. That time is less than the 100-ms window for the motherboard. When the timing circuit times out, the control logic 304 controls the operation of transistors Q2, Q3, Q4 and Q5 to switch the 5 volt and 3.3 volt dual outputs from their standby voltage input to the line voltages from the power supply 10.

The circuit 22 simplifies the implementation of ACPI-compliant designs in microprocessor and computer applications. The circuit 22 (representative of an entire family of power mangement circuits) integrates two linear controllers and a low-current pass transistor, as well as the monitoring and control functions into a 16-pin SOIC package. One linear controller 305 generates the 3.3V DUAL voltage plane from an ATX power supply's

5VSB output during sleep states S3, S4/S5), powering the PCI slots, and other peripherals, through an external pass transistor, as instructed by the status of the 3.3V DUAL enable pin. An additional pass transistor is used to switch in the ATX 3.3V output for operation of this output during S0 and S1 (active) operating states. The second linear controller 306 supplies the computer system's 2.5V/3.3V memory power through an external pass transistor in active states. During S3 state, an integrated pass transistor supplies the 2.5V/3.3V output sleep-state power. A third controller 307 powers up a 5V DUAL plane by switching in the ATX 5V output in active states, or the ATX 5VSB in sleep states.

The operating mode of circuit 22 (active-state outputs or sleep-state outputs) is selectable through two control pins: 319 and 318. Further control of the logic 304 governing activation of different power modes is offered through two enabling pins: 319 and 320. In active states, the 3.3V DUAL linear regulator 305 uses an external N-channel pass MOSFET 331 to connect the output 314 (V OUT1) directly to the 3.3V input supplied by an ATX (or equivalent) power supply, while incurring minimal losses. In sleep state, the 3.3V DUAL output is supplied from the ATX 5VSB 312 through an NPN transistor 330, also external to the controller. Active state power delivery for the 2.5/3.3V MEM output 351 is done through an external NPN transistor 332, or an NMOS switch for the 3.3V setting. In sleep states, conduction on this output is transferred to an internal pass transistor. The 5V DUAL output 352 is powered through two external MOS transistors. In sleep states, a PMOS (or PNP) transistor 333 conducts the current from the ATX 5VSB output, while in active states, current flow is transferred to an NMOS transistor 334 connected to the ATX 5V output. Similar to the 3.3V DUAL output, the operation of the 5V DUAL output 352 is dictated not only by the status of the 317 and 318 pins, but that of the EN5VDL enable pin 319 as well.

A 5VSB power on reset (POR) signal initiates a soft-start sequence. An internal 10 μA current source charges an external capacitor to approximately 2.8V. Error amplifiers reference inputs are clamped to a level proportional to the soft-start pin voltage. As the soft-start pin voltage slews from about 1.25V to 2.5V, the input clamp allows a rapid and controlled output voltage rise.

Figure 4 shows the soft-start sequence for the typical application start-up in a sleep state with all output voltages enabled. At time TO 5V SB (bias) is applied to the circuit. At time T1, 5V SB surpasses POR level and an internal fast charge circuit quickly raises the SS capacitor voltage to approximately 1V. At this point, the 10μA current source continues to charge the capacitor up to T2, where a voltage of 1.25V(typically) is reached and an internal clamp limits further charging. Clamping of the soft-start voltage (T2 to T3 interval) should only be observed with capacitors smaller than 0.1μF. Soft-start capacitors of 0.1μF and above should present a soft-start ramp void of this plateau. At time T3, 3ms (typically pas the 5V SB POR (T1), the 10μA current source resumes charging the soft-start capacitor. At this point, the error amplifiers' reference inputs are starting their transitions, causing the output voltages to ramp up proportionally. The ramping continues until time T4 when all the voltages reach the set value. At time T5, when the soft-start capacitor value reaches approximately 2.8V, the under-voltage monitoring circuits are activated and the soft-start capacitor is quickly discharged down to the value attained at time T2 (approximately 1.25V).

If both 317 and 318 are logic high at the time the 5VSB is applied, the circuit 22 will assume an active state and keep off the controlled external transistors until about 50 ms after the ATX's 12V output (sensed at the 12V input 311) exceeds the set threshold (typically 10.8V). This timeout feature is necessary in order to insure the main ATX outputs are stabilized. The timeout also assures smooth transitions from sleep into active when sleep states are being supported.

During sleep to active state transitions from conditions where the outputs are initially 0V (such as S4/S5 to S0 transition with EN3VDL = 1 and EN5VDL = 0, or simple power-up sequence directly into active state), the 3V DUAL and 5V DUAL outputs go through a quasi soft-start by being pulled high through the body diodes of the N-channel MOSFETs connected between these outputs and the 3.3Vand 5V ATX outputs, respectively, Figure 5 shows this start-up scenario.

5V SB is already present when the main ATX outputs are turned on at a time T0.

Similarly, the soft-start capacitor has already been charged up to 1.25V and the clamp is active, awaiting for the 12V power-on reset (POR) timer to expire. As a result of 3.3V IN and 5V IN ramping up, the 3.3V DUAL and 5V DUAL output capacitors C1, C3 charge up through the body diodes of Q3 and Q5, respectively (see Figure 3). At time T1, the 12V ATX output exceeds the 12V undervoltage threshold of circuit 22, and the internal 50ms (typical) timer 25 (Fig. 2) is initiated. At T2 the time-out initiates a soft-start, and the memory output is ramped-up, reaching regulation limits at time T3. Simultaneous with the memory voltage ramp-up, the DLA output 321 is pulled high (to 12V), turning on Q3 and Q5, and bringing the 3.3V DUAL and 5V DUAL outputs in regulation at time T2. At time T4, when the soft-start voltage reaches approximately 2.8V, the undervoltage monitoring circuits are enabled and the soft-start capacitor is quickly discharged to approximately 2.45V.

Requests to go into a sleep state during an active state soft-start ramp-up result in a chip reset, followed by a new soft-start sequence into the desired state.

Having thus disclosed the preferred embodiment of the invention, those skilled in the art will appreciate that further modifications, changes and omissions of one or more elements to the preferred embodiment may be made without departing from the spirit and scope of the invention.

Claims:

1. An integrated circuit for monitoring and controlling multiple power outputs from a power supply that generates a primary power voltage and one or more secondary power voltages derived from the primary power voltage, comprising:

input means for receiving the primary and secondary power voltages from the power supply;

means for controlling the primary and secondary power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the primary power voltage to a reference signal;

means for sensing when the primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the primary and secondary power voltages to the controlled voltage power outputs for a selected delay time after the primary power voltage reaches the reference threshold level.

2. The integrated circuit of claim 1 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

3. The integrated circuit of claim 1 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the primary power voltage and to the comparator.

4. The integrated circuit of claim 3 wherein the delaying means comprises a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the input power supply voltages to the controlled outputs for the selected delay time.

5. The integrated circuit of claim 1 further comprising a linear controller for controlling the output voltage of each of the power output voltages of the power monitor circuit.

6. A computer system with monitored power comprising in combination:

a power supply for generating a primary dc power voltage and one or more secondary dc power voltags derived from the primary dc power output, a motherboard comprising multiple units inlcuding a memory unit and a central processing unit, wherein said uits may require different operating voltages; and a power monitoring integrated circuit disposed between the power supply and the motherboard for controlling supply of power from the power supply to the motherboard, said power monitoring circuit comprising

input means for receiving the primary and secondary power voltages from the power supply;

means for controlling the receviced power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the primary power voltage to a reference signal;

means for sensing when the primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the controlled power output voltages to the computer for a selected delay time after the primary power voltage reaches the reference threshold level.

7. The computer system of claim 6further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

8. The computer system of claim 6 wherein the means for comparing comprises a voltage divider and a comparator, wherein the comparator is coupled to a threshold reference voltage and the voltage divider is coupled to the primary power voltage and to the comparator.

9. The computer system of claim 8 wherein the delaying means comprises a timing circuit and the output of the comparator is coupled to the timing circuit for delaying connection of the controlled power output voltages to the computer for the selected delay time.

10. The computer system of claim 6 wherein the means for controlling the output voltages

comprises a plurality of linear controllers with each linear controller controlling the output voltage of one of the power output voltages of the power monitor circuit.

11. A method for monitoring and controlling power from a power supply that generates a primary power voltage and one or more secondary power voltages derived from the power voltage, comprising:

receiving the primary and secondary power voltages from the power supply;

controlling the received power voltages to generate controlled voltage power outputs

comparing a signal representative of the primary power voltage to a reference signal;

sensing when the primary power output voltage reaches or exceeds a threshold reference level; and

delaying connection of the power supply contolled voltage power outputs for a selected delay time after the input power supply reaches the reference threshold level.

12. The method of claims 11 further comprising generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a useable and effective voltage level.

13. The method of claims 11 the step of comparing comprises voltage dividing a signal representative of the primary power voltage and comparing the voltage divided signal to a threshold reference voltage.

14. The method of claims 11 wherein the delaying step comprises timing an interval starting when the voltage divided signal exceeds the threshold reference signal and delaying connection of the contolled voltage power outputs to the computer for a selected delay time.

15. The method of claims 11 further comprising linearly controlling each of the power output voltages of the power monitor circuit.

ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

ABSTRACT

A power monitor circuit and method delays the start of a computer until multiple power lines are at a safe level of operation. The integrated circuit monitors only the voltage of a primary power supply output and eliminates the need for monitor circuits on each supply output. The power supply is made to exacting specifications that tie the 5 volt and 3.3 volt supplies to the primary 12 volt supply. The ATX power supply drives the 3.3 and 5.0 supplies to reach 90% of their values within 40 ms after the 12 volt supply reaches 90% of its value. A time delay circuit 25 delays switching the 3.3 and 5 volt dual outputs from the standby voltage supply to the active voltage supplies until after the primary 3.3 and 5 volt are at a safe operating level.

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Serial No. **TBA**	Filing Date **Herewith**	Examiner **Unknown**	Group Art Unit **Unknown**

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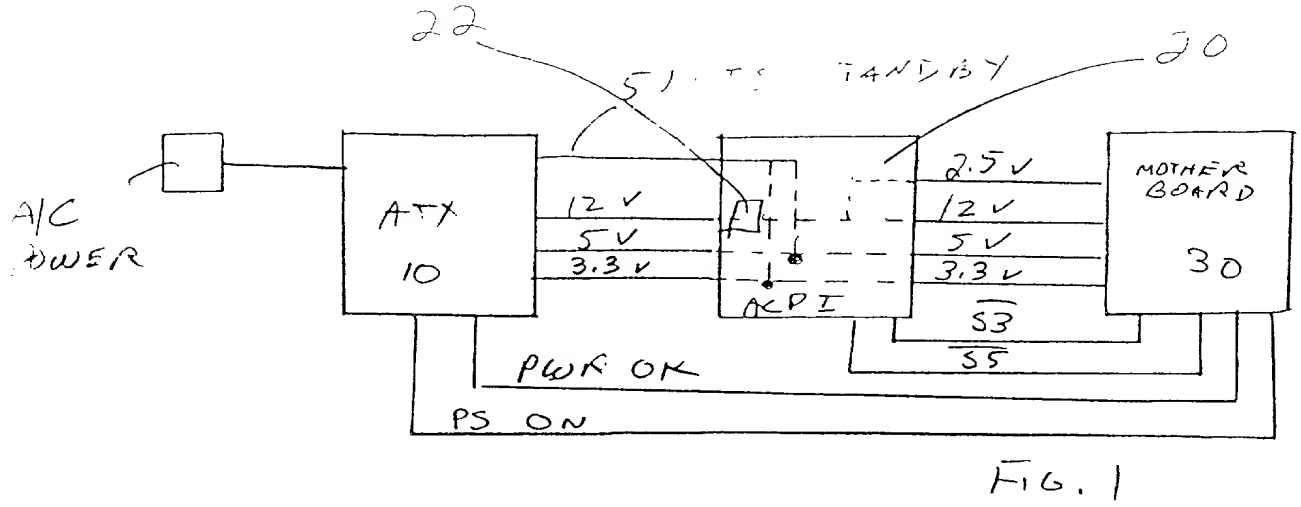
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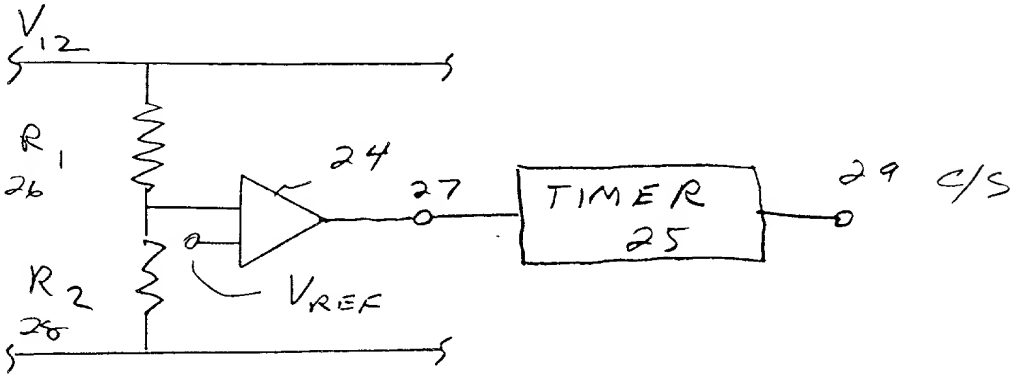
FIG. 1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R_2
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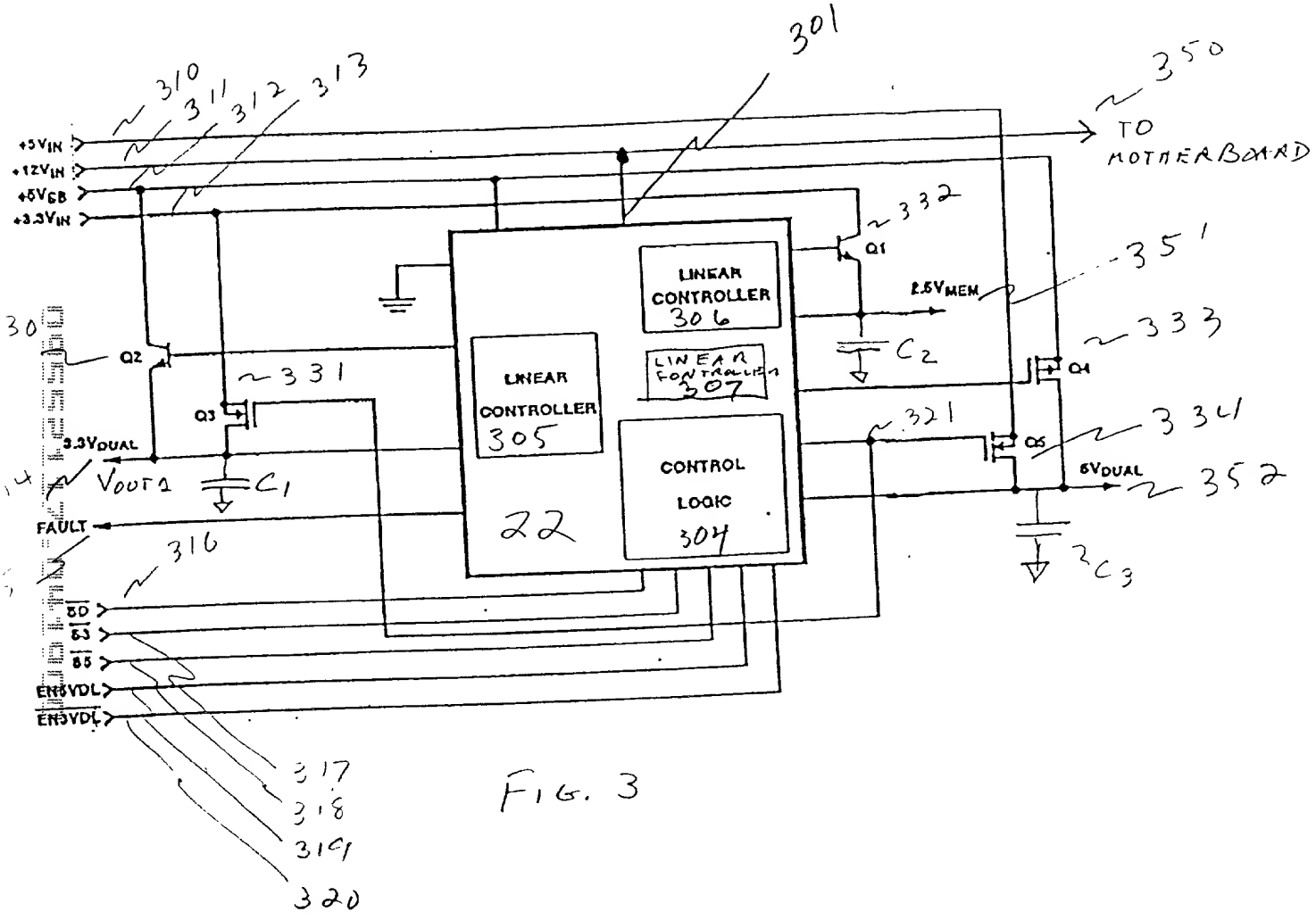
FIG. 2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LINEAR CONTROLLER 307
CONTROL LOGIC 304
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Q1
Q2
Q3
Q4
Q5
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331
333
321
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VOUT2
C1
C2
C3
351
352
5VDUAL
FAULT
316
SD
S3
S5
EN5VDL
EN3VDL
317
318
319
320

FIG. 3

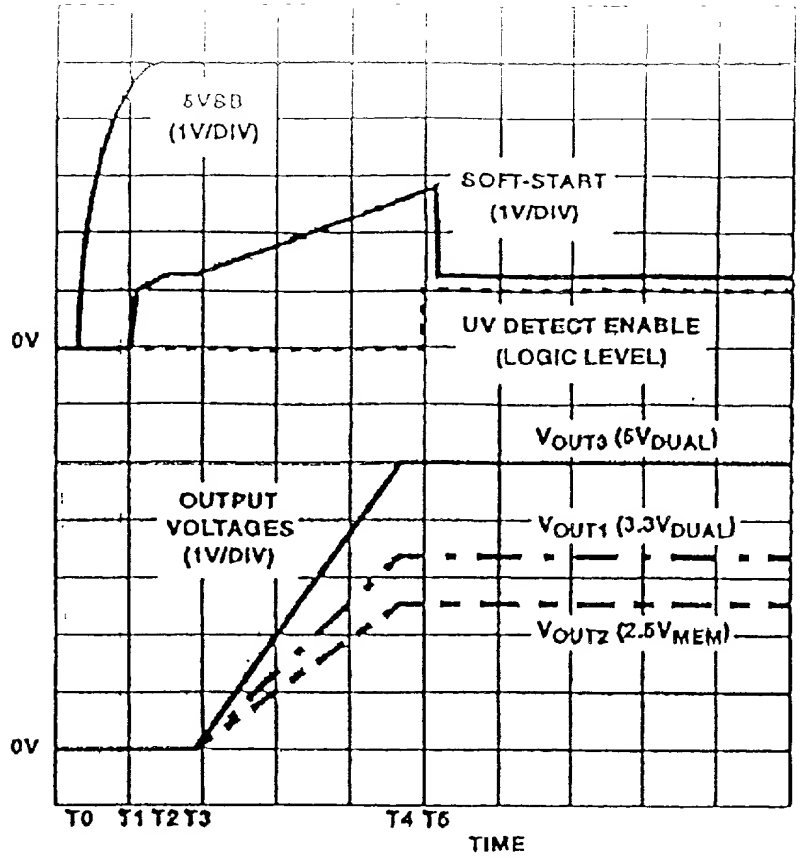

FIGURE 4 SOFT-START INTERVAL IN A SLEEP STATE (ALL OUTPUTS ENABLED)

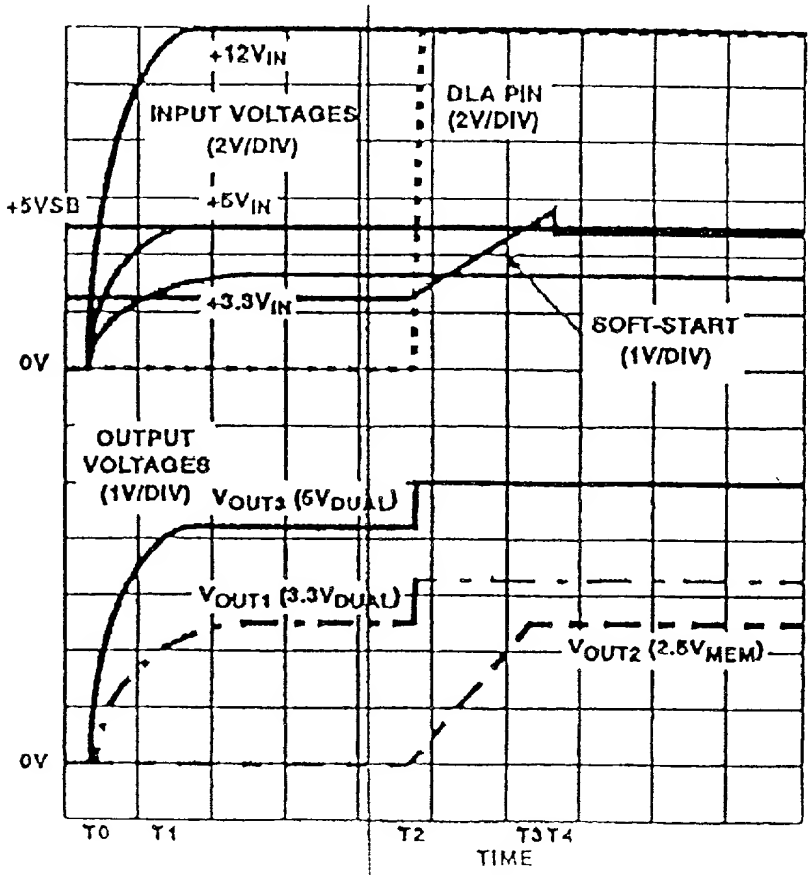

FIGURE 5 SOFT-START INTERVAL IN AN ACTIVE STATE

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	87552.070100/SE-1486IP.A
First Named Inventor	Bogdan M. Duduman
COMPLETE IF KNOWN	
Application Number	TBA
Filing Date	Herewith
Group Art Unit	Unknown
Examiner Name	Unknown

As a below named inventor, I hereby declare

My residence, post office address, and citizenship are as stated below next to my name

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) _____ as United States Application Number or PCT International

Application Number TBA and was amended on (MM/DD/YYYY) _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1 56

I hereby claim foreign priority benefits under 35 U S C 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
None			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

I hereby claim the benefit under 35 U S C 119(e) of any United States provisional application(s) listed below

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/130,828	April 23, 1999	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U S C 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U S C 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
None		

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Name	Registration Number	Name	Registration Number
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Lee J. Fleckenstein	36,136	Laurence S. Roach	45,044
Ronald J. Kisicki	38,205	Douglas A. Balog	42,288
Bidyut K. Niyogi	27,071	Joseph W. King, Jr.	35,768

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] *OR* ☒ Correspondence address below

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U S C 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Bogdan M.	Duduman

Inventor's Signature	B. Duduman					Date	04/18/2000
Residence: City	Raleigh	State	NC	Country	USA	Citizenship	USA
Post Office Address	6501 Golden Lantern Court, Apt. 207						
Post Office Address							
City	Raleigh	State	NC	ZIP	27613	Country	USA

☐ Additional inventors are being named on the ____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Bogdan M. Duduman**			Docket No. **87552.070100/SE-1486-IP.A**
Serial No. **TBA**	Filing Date **Herewith**	Examiner **Unknown**	Group Art Unit **Unknown**

Invention: **ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS**

jc525 U.S. PTO
09/551117
04/19/00

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